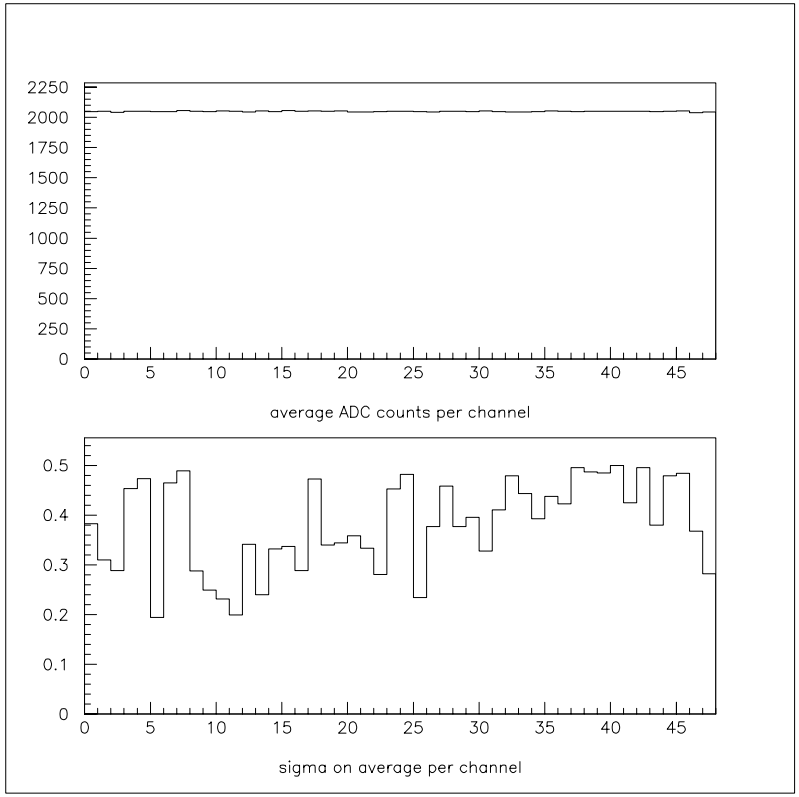
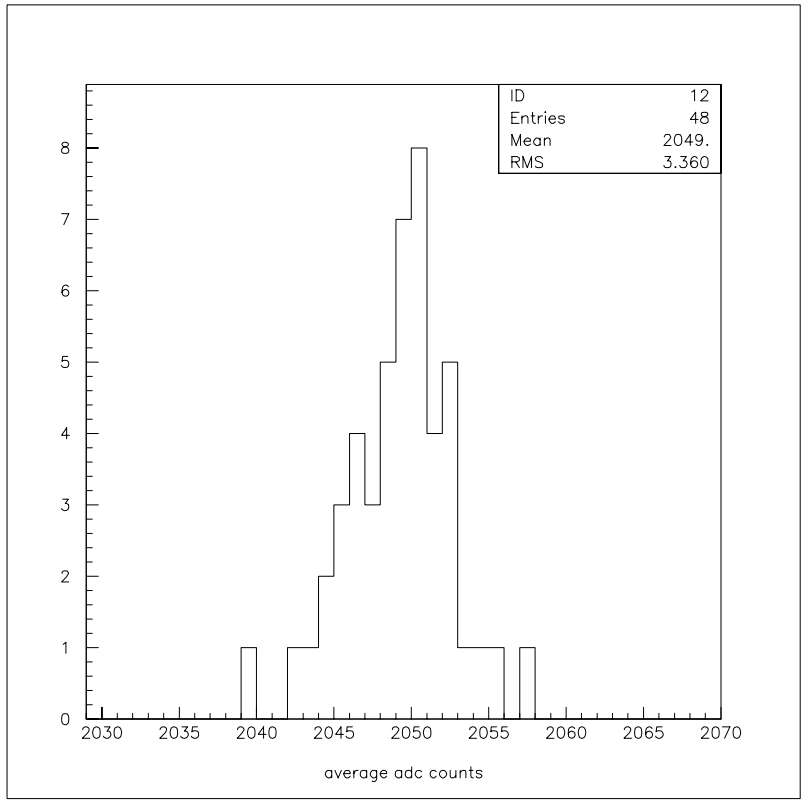
ADC board performance without input





Top: Average ADC counts vs. channel number
Bottom: Sigma on the average vs. channel number

Distribution of average ADC counts in 48 channels

Few other items

- The serial data from the ADC is running 720 MBits per sec, ~1.4ns clock.
  - We can adjust the phase between the clock and data in 8 steps, 45 degree per step.
  - We verify there is at least 700ps, 180 degree, of timing margin in the receiver's timing window.
- We are currently fabricating a test board to host 6 preamp to test the front-end performance of the ADC board.